Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A circuit protected against transient disturbances, the circuit comprising:

a combinatory logic circuit ~~(10)~~ having at least one output ~~(A),~~ ;

a circuit ~~(20, 11)~~ for generating an error control code for said output; and

a memory element ~~(24,24')~~ arranged at said output, controlled by the error control code generation circuit to be transparent when the error control code is correct, and to keep ~~its~~ the state of said output unchanged when the error control code is incorrect.

Claim 2 (Currently Amended): The protected circuit of claim 1, wherein the error control code generation circuit includes a circuit ~~(20)~~ for calculating a parity bit ~~(P)~~ for said output ~~(A)~~ and a circuit ~~(22)~~ for checking the parity of the output and of the parity bit.

Claim 3 (Currently Amended): The protected circuit of claim 1 wherein the error control code generation circuit includes a duplicated logic circuit ~~(11)~~, said memory element ~~(24)~~ being provided to be transparent when the outputs of the logic circuit ~~(10)~~ and of the duplicated circuit ~~(11)~~ are identical, and to keep its state when said outputs are different.

Claim 4 (Currently Amended): The protected circuit of claim 1, wherein the error control code generation circuit includes an element ~~(90)~~ for delaying said output by a predetermined duration greater than the maximum duration of transient errors, said memory element ~~(24')~~ being provided to be transparent when the outputs of the logic circuit and of the delay clement are identical, and to keep its state when said outputs are different.

SILICON VALLEY
ATENT GROUP LLP

0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

Claim 5 (Currently Amended): The protected circuit of claim 3, wherein said memory element ~~(24)~~ is formed from a logic gate providing said output of the logic circuit, this logic gate including at least two first transistors ~~(MN 1, MP2)~~ controlled by a signal ~~(a)~~ of the logic circuit and at least two second transistors ~~(MP1, MN2)~~ controlled by the corresponding signal ~~(a*)~~ of the duplicated circuit, each of the second transistors being connected in series with a respective one of the first transistors.

Claim 6 (Currently Amended): A circuit protected against transient disturbances, the circuit comprising:

a combinatory logic circuit ~~(10)~~ having at least one output ~~(A)connected to~~;

a first ~~synchronization~~ flip-flop ~~(70, 92)~~ rated by a clock ~~(CK)~~, the first flip-flop being connected to receive said output;

a second flip-flop ~~(71, 93)~~ connected to said output and rated by the clock delayed by a predetermined duration ~~(δ)~~; and

a circuit ~~(74,95)~~ for analyzing the outputs of the flip-flops, the analysis circuit ~~(95)~~ indicating an error if the flip-flop outputs are different.

Claim 7 (Currently Amended): The protected circuit of claim 6, wherein the second flip-flop ~~(93)~~ is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock.

Claim 8 (Currently Amended): A circuit protected against transient disturbances, the circuit comprising:

a combinatory logic circuit ~~(10)~~ having at least one output ~~(A)connected to~~;

a first ~~synchronization~~ flip-flop ~~(70)~~ rated by a clock ~~(CK)~~, the first flip-flop being connected to receive said output;

a second flip-flop ~~(71)~~ rated by the clock and receiving said output delayed by a predetermined duration ~~(δ),~~; and

a circuit ~~(74)~~ coupled to receive the outputs of the first flip-flop and the second flip-flop, for analyzing the flip-flop outputs, the analysis circuit indicating an error if the flip-flop outputs are different.

SILICON VALLEY
ATENT GROUP LLP
0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

Claim 9 (Currently Amended): A circuit protected against transient disturbances, the circuit comprising:

three identical logic circuits ~~(10a, 11a 10b)~~, wherein each of the logic circuits is preceded by a two-input memory element ~~(24a, 24b, 24c)~~ respectively receiving the outputs of the two other logic circuits, each memory element being provided to be transparent when its two inputs are identical, and to keep its state unchanged when the two inputs are different.

Claim 10 (Previously presented): The protected circuit of claim 9, wherein the logic circuits are inverters and the memory elements include, in series, two P-channel MOS transistors and two N-channel MOS transistors, a first one of the inputs of the memory element being connected to the gates of a first one of the P-channel MOS transistors and of a first one of the N-channel MOS transistors, and the second input of the memory element being connected to the gates of the two other transistors.

Claim 11 (new): The protected circuit of claim 8 further comprising:

a third flip-flop rated by the clock and receiving said output delayed by twice the predetermined duration;

wherein the analysis circuit is further coupled to receive the output of the third flip-flop.

SILICON VALLEY
ATENT GROUP LLP

0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210